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# DATA SHEET

# TEA1541
SMPS control IC with synchronization function

Product specification

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Philips Semiconductors

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## 1 FEATURES

### 1.1 Distinctive features

- Universal mains supply operation (70 to 276 V AC)
- High-level of integration requiring few external components
- Synchronization with internal frequency divider
- Frequency independent over-power protection.

### 1.2 Green features

- Frequency reduction at low power standby for improved system efficiency (<3 W)
- Burst mode operation for very low power standby levels (<1 W)
- On-chip start-up current source.

### 1.3 Protection features

- Safe restart mode for system fault conditions
- Continuous mode protection using demagnetization detection (zero switch-on current)
- Accurate and adjustable overvoltage protection
- Winding short-circuit protection
- Undervoltage protection (foldback during overload)
- Overtemperature protection
- Adjustable low overcurrent protection (OCP) trip level
- Soft (re)start
- Mains voltage-dependent operation-enabling level.

## 2 GENERAL DESCRIPTION

The TEA1541 is a second generation GreenChip™(1) Switched Mode Power Supply (SMPS) controller IC that operates directly from the rectified universal mains.
A high-level of integration provides a cost-effective power supply requiring only a few external components.

The TEA1541 controller enables easy design of highly efficient, reliable switched mode power supplies.
Its internal oscillator can be synchronized to pulses from an external signal source. External synchronizing pulses whose frequency is above the SMPS switching frequency range are divided by an internal divider.

Special built-in green functions ensure optimum efficiency at all power levels. At low power (standby) levels, the SMPS supply operates at a lower frequency. In burst standby mode, power consumption can be reduced to less than 1 W.

The proprietary EZ-HV SOI process allows start-up directly from the rectified mains voltage, avoiding the need for bleeder circuits, and also saves energy.

A low voltage BICMOS implements accurate control and high speed protection functions.

(1) GreenChip is a trademark of Koninklijke Philips Electronics N.V.

## 3 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| TEA1541P | DIP8 | plastic dual-in-line package; 8 leads (300 mil) | SOT97-1 |

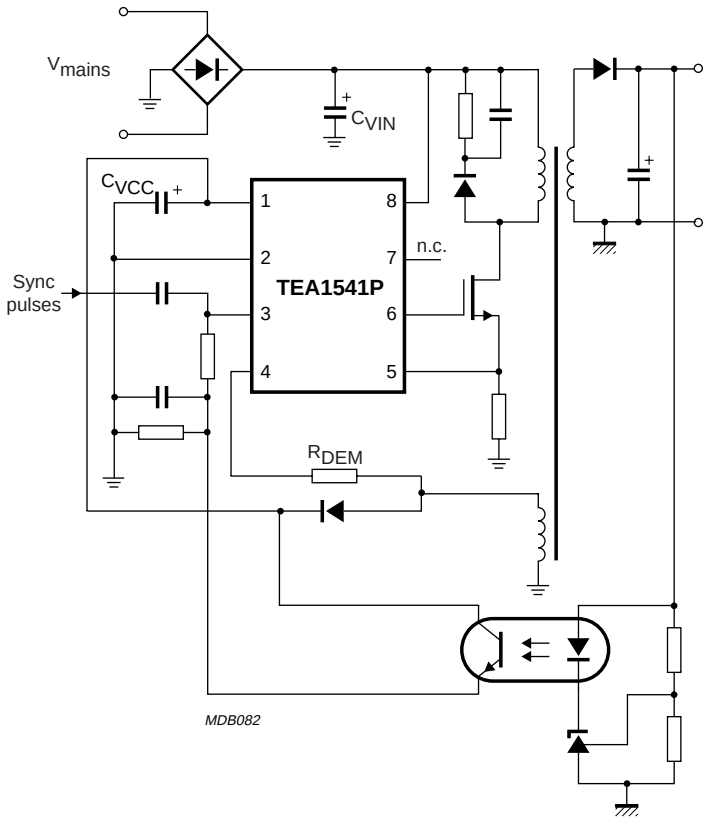



Fig.1 Basic application.

## 4 BLOCK DIAGRAM

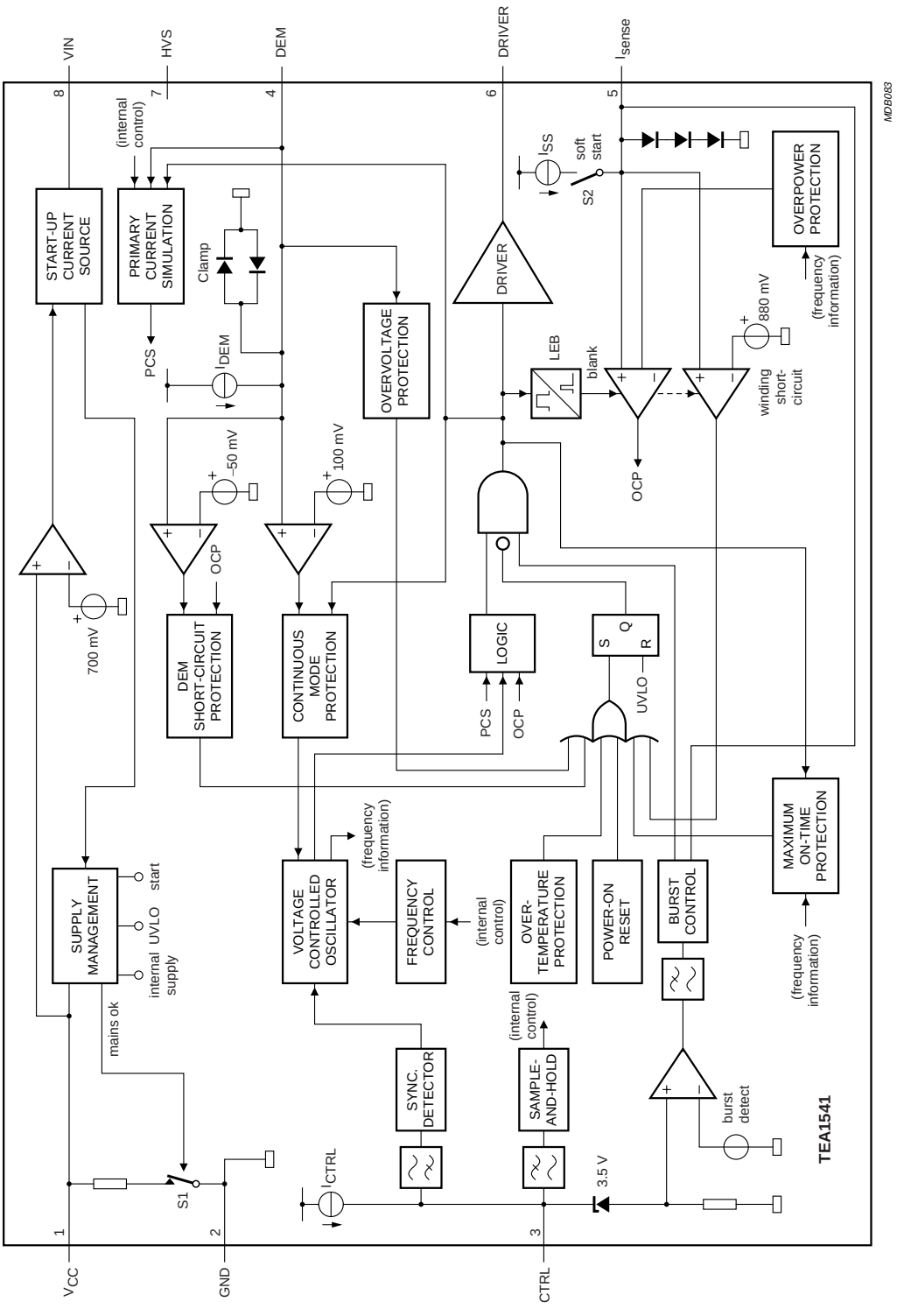



Fig.2 Block diagram.

## 5 PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| $V_{CC}$ | 1 | supply voltage |
| GND | 2 | ground |
| CTRL | 3 | control input |
| DEM | 4 | input from auxiliary winding for demagnetization timing, OVP and overpower protection (OPP) |
| $I_{sense}$ | 5 | programmable current sense input |
| DRIVER | 6 | gate driver output |
| HVS | 7 | high voltage safety spacer, not connected |
| VIN | 8 | input for start-up current and mains voltage recognition |

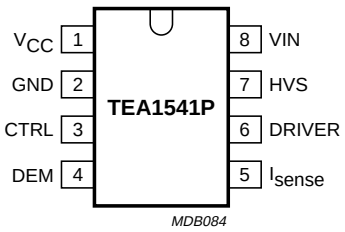



Fig.3 Pin configuration.

## 6 FUNCTIONAL DESCRIPTION

The TEA1541 is intended as the controller for a compact flyback converter for CRT monitor applications. The IC is situated on the primary side of the output transformer. Output power is determined by the current in the primary winding. The voltage across an auxiliary winding in the transformer is converted to a current by resistor $R_{DEM}$ and used by the IC to derive the current in the primary winding. This winding is also used for continuous mode protection, overvoltage protection, and to power the IC after start-up.

The IC can operate in either synchronized or unsynchronized mode. In synchronized mode, the IC synchronizes the converter switching frequency to the monitor line frequency to prevent interference.
Line synchronizing pulses are applied to pin CTRL.

Each operating cycle of the converter comprises a primary stroke followed by a secondary stroke. During the primary stroke, current flows in the primary winding.
The secondary stroke transfers the energy stored in the transformer core to the secondary winding. In either synchronized or unsynchronized mode, the primary stroke only starts at the end of the secondary stroke when the transformer is demagnetized to ensure zero switching primary current. If no synchronizing pulses are present (unsynchronized mode), the IC will operate at its minimum switching frequency.

The IC has an internal frequency divider which allows it to operate in synchronized mode at a lower frequency than the synchronizing pulses supplied to pin CTRL by the application. The limited frequency range allows an economical design of the transformer.

In unsynchronized mode, when the power that is drawn from the converter decreases, the converter switching frequency also decreases. At very low power (standby) levels, the frequency of the VCO decreases from 25 kHz to the minimum value of approximately 6 kHz as shown by the slope of Fig.4. In a typical application it is possible to obtain an input power of less than 3 W with an output power of 100 mW.

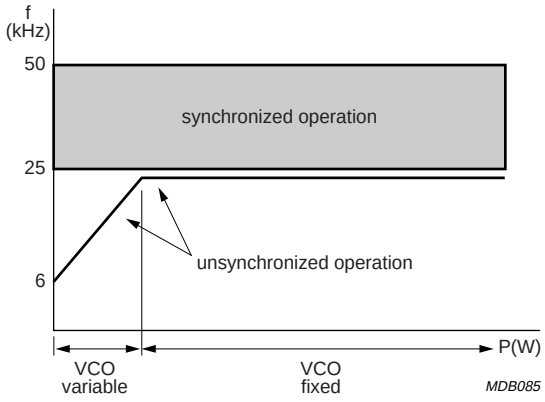



Fig.4 Multi mode operation.

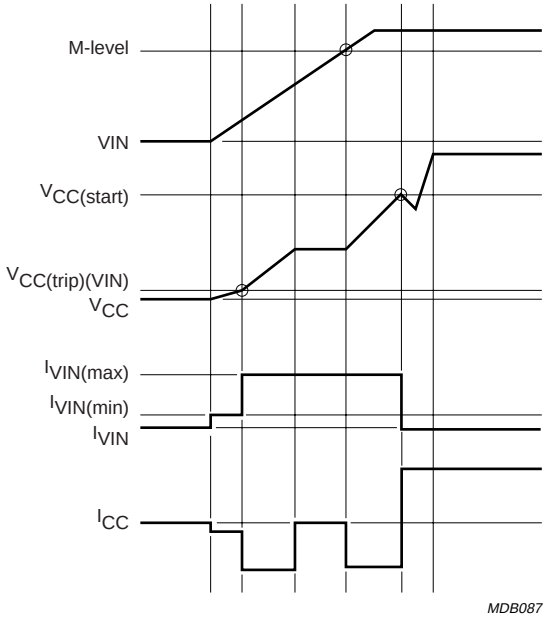



Fig.5 Start-up sequence.

### 6.1 Start-up, mains voltage-dependent operation-enabling level and undervoltage lock-out

Initially, the IC is supplied by the rectified mains voltage at pin VIN. When the voltage at pin $V_{CC}$ is below the $V_{CC}$ voltage for VIN current trip level $V_{CC(trip)(VIN)}$, the supply current drawn from pin VIN, ($I_{VIN}$) is at the low value $I_{VIN(min)}$. When $V_{CC}$ rises to the $V_{CC(trip)(VIN)}$ level, the current at pin VIN changes to the high value $I_{VIN(max)}$. When the voltage at pin VIN is below the mains voltage-dependent operation-enabling level (M-level), the IC supply capacitor $C_{VCC}$ is charged by the internal start-up current source to approximately 5 V. When the voltage at pin VIN exceeds the M-level, the start-up current source continues to charge $C_{VCC}$ (switch S1 open; see Fig.2).

When $V_{CC}$ reaches the start-up voltage level $V_{CC(start)}$, the IC switches to high efficiency (green function) operation by no longer drawing current from pin VIN (see Fig.5).

At $V_{CC(start)}$ the IC activates the external MOSFET. When the voltage across the auxiliary winding rises above the voltage across $C_{VCC}$, the IC supply current will be supplied by the auxiliary winding via pin $V_{CC}$.

If the voltage on pin $V_{CC}$ falls below the $V_{CC}$ undervoltage lock-out level $V_{CC(UVLO)}$, the IC stops switching and enters a safe restart mode in which current to the IC is supplied by the rectified mains voltage via pin VIN, and $C_{VCC}$ is re-charged by the internal start-up current source to $V_{CC(start)}$.

Inhibiting the auxiliary supply by external means causes the converter to operate in a stable, well-defined burst mode. This is a burst standby mode that is less efficient than the normal burst standby mode described in section 6.12.

If the voltage at pin VIN falls below the mains undervoltage lock-out level $M_{UVLO}$, a safe restart mode is activated, and the IC stops switching.

During normal operation (non-burst standby mode), the duty cycle of the IC, and thus the output power of the supply, is regulated by a control voltage at pin CTRL.

If pin $V_{CC}$ is connected to ground, the IC switches to low power standby operation and the start-up current drawn via pin VIN reduces to 400 μA (typical). When the voltage on pin $V_{CC}$ rises above 700 mV (typical), the start-up current increases to 1 mA (typical).

### 6.2 Supply management

All internal reference voltages are derived from a temperature compensated, on-chip bandgap.

### 6.3 Primary current regulation

The IC uses current mode control for its good line regulation behaviour. The primary current is sensed indirectly via the voltage at pin DEM.

The 'on-time' of the external MOSFET is controlled by the voltage on pin CTRL which is compared with the internal simulated primary current information. For pin CTRL voltages ($V_{CTRL}$) between 1 and 1.6 V, the on-time is calculated by the equation:

$$t_{on} = \alpha_{PCS} \times \left( \frac{1.6 - V_{CTRL}}{I_{DEM}} \right) [ns]$$

where:

- $t_{on}$: the on-time
- $\alpha_{PCS}$: an internal constant which is approximately 0.9.
- $V_{CTRL}$: the voltage on pin CTRL
- $I_{DEM}$: the current drawn from pin DEM during the primary cycle.

### 6.4 Oscillator

In synchronized mode, the switching frequency of the SMPS $f_{smps}$ is controlled by the synchronizing pulses $f_{sync}$ at pin CTRL. Synchronized mode prevents noise disturbance on the CRT monitor screen. Synchronizing pulses whose frequency is outside of the $f_{osc}$ and $f_{smps(max)}$ window of 26 to 54 kHz are divided by an internal frequency divider. A small frequency hysteresis exists to ensure a stable frequency switch-over. In unsynchronized mode, the system runs at $f_{osc}$ (26 kHz). In unsynchronized mode, at very low power (standby) levels, the frequency of the VCO and consequently the SMPS switching frequency is reduced linearly to its low value of approximately 6 kHz (see Figs 4 and 6).

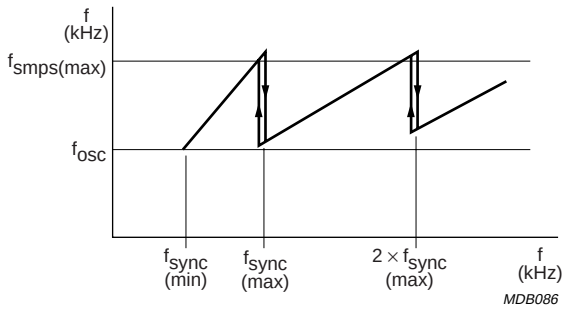



Fig.6 Switching frequency as a function of the synchronizing frequency.

### 6.5 Demagnetization

The system always operates in discontinuous conduction mode to ensure demagnetization of the output transformer core. A primary cycle only starts when the secondary cycle has ended.

Pin DEM protects against an output short-circuit on a cycle-by-cycle basis, by immediately lowering the switching frequency to give a longer off-time and a lower operating power.

Demagnetization detection is suppressed automatically at the start of each secondary cycle for a period $t_{suppr}$. Suppression of demagnetization detection is necessary for applications where the transformer has a large leakage inductance, at low output voltages and at start-up.

If, due to a fault condition, pin DEM is left open circuit, operation of the flyback converter supply immediately stops, and restarts when the fault situation is removed and pin DEM is reconnected.

If, during start-up, a fault condition causes pin DEM to be shorted to ground, operation of the flyback converter supply stops after the first cycle, and the IC then begins a restart cycle. This situation continues until the short-circuit is removed. Short-circuit protection is also active at full power to ensure limitation of peak current.

### 6.6 Minimum and maximum 'on-time'

The minimum on-time of the converter is not limited by the leading edge blanking time, and therefore can be zero.

The IC limits the maximum on-time to $\frac{1}{f_{smps}}$

where $f_{smps}$ is the converter switching frequency in either synchronized or unsynchronized mode. If the system requires a longer on-time, a fault condition is assumed, for example, if $C_{VIN}$ is removed, the IC will stop switching and enter the safe restart mode.

### 6.7 Overvoltage protection

The TEA1541 allows OVP to be set accurately.
The flyback converter output voltage is accurately represented by the voltage across the auxiliary winding. The auxiliary winding voltage is monitored by the current flowing into pin DEM during the demagnetizing cycle of the transformer. The inevitable voltage spikes at pin DEM are reduced using an internal filter.

If the output voltage causes the current into pin DEM to exceed the OVP level $I_{OVP(DEM)}$, the OVP circuit turns off the power MOSFET. The controller then waits until the $V_{CC(UVLO)}$ condition is reached. This is followed by a safe restart cycle, before switching recommences.
This process is repeated until the OVP condition ends.

The output voltage at which OVP activates, $V_{o(ovp)}$ is set by the value of resistor, $R_{DEM}$, (see Fig.8) using the equation:

$$V_{o(ovp)} = \frac{N_s}{N_{aux}} \times (I_{OVP(DEM)} \times R_{DEM} + V_{clamp(DEM)(pos)})$$

where N is the number of turns on the transformer windings; $V_{clamp(DEM)(pos)}$ is the positive clamp voltage on pin DEM; reference current $I_{OVP(DEM)}$ is set internally.

### 6.8 Overcurrent protection and overpower protection

The current in the transformer primary is measured accurately by the internal cycle-by-cycle source current limit circuit using the external sense resistor $R_{sense}$.
The accuracy of the current limit circuit allows the transformer core to have a minimum specification for the output power required. The OCP circuit limits the 'sense' voltage to an internal level, and is activated after the leading edge blanking period, $t_{leb}$ generated by the Leading Edge Blanking circuit (LEB shown in Fig.2). Leading edge blanking is required to inhibit OCP for a short period when the power MOSFET turns on. This ensures that the MOSFET is not turned off prematurely due to the false sensing of an overcurrent condition caused by current spikes produced by the discharge of primary-side snubber and parasitic capacitances.

The OCP level is adjusted proportionally to the switching frequency such that the product of $(I_{peak})^2 \times$ frequency stays constant. This arrangement also implements OPP, ensuring that the maximum output power is independent of the switching frequency, otherwise the output power would increase in direct proportion to the switching frequency.

### 6.9 Soft start

The soft start function allows the transformer peak current to slowly increase at every start-up and restart, to prevent transformer rattle.

The soft start function requires a resistor $R_{SS}$ and capacitor $C_{SS}$ to be connected between pin $I_{sense}$ and the sense resistor $R_{sense}$ (see Fig.7). $C_{SS}$ is charged by an internal current source $I_{SS}$ to $V = I_{SS} \times R_{SS}$, to a maximum of approximately 0.5 V.

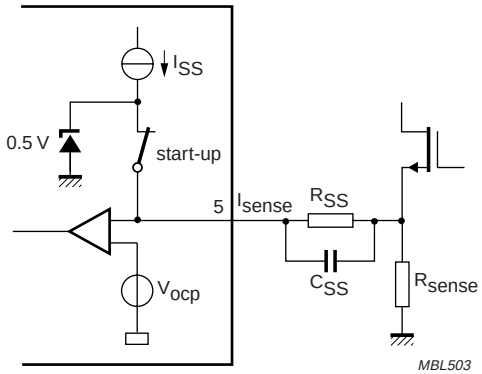



Fig.7 Soft start.

The rate at which the primary current increases can be adjusted by changing the values of $R_{SS}$ and $C_{SS}$ to change the circuit time constant: $\tau = R_{SS} \times C_{SS}$

The maximum primary current is calculated by the equation: $I_{primary(max)} = \frac{V_{sense(max)} - (I_{SS} \times R_{SS})}{R_{sense}}$

where $V_{sense(max)}$ is the maximum source voltage for OCP. $I_{SS}$ flows when the voltage on pin $I_{sense}$ is less than approximately 0.5 V. If this voltage exceeds 0.5 V, the soft-start current source starts to limit $I_{SS}$ and completely switches $I_{SS}$ off at $V_{CC(start)}$.

Note that $I_{SS}$ is derived from the internal current source supplying charging current to pin $V_{CC}$. During soft-start, the charging current to pin $V_{CC}$ will be reduced by up to 60 μA depending on the value of $R_{SS}$.

### 6.10 Winding short-circuit protection

The winding short-circuit protection circuit is activated after the leading edge blanking period. A short-circuit in the transformer winding is detected when the voltage at pin $I_{sense}$ exceeds the winding short-circuit protection voltage $V_{swp}$. When a short-circuit is detected, the flyback converter supply will stop switching. When the voltage at pin $V_{CC}$ falls below $V_{CC(UVLO)}$, the IC enters safe restart mode, and capacitor $C_{VCC}$ will recharge via the internal start-up current source supplied from pin VIN until the flyback converter supply restarts at $V_{CC(start)}$. The fault detection and restart cycle will be repeated until the short-circuit is removed. The winding short-circuit protection circuit also provides protection if a diode in the transformer secondary circuit goes short-circuit.

### 6.11 Overtemperature protection

An accurate temperature protection circuit stops the converter from switching if the IC junction temperature exceeds the maximum temperature protection level $T_{prot(max)}$. When the voltage at pin $V_{CC}$ falls below $V_{CC(UVLO)}$, the IC enters safe restart mode, and capacitor $C_{VCC}$ will recharge to $V_{CC(start)}$ via the internal start-up current source derived from pin VIN. If the temperature is still too high, the voltage at pin $V_{CC}$ will fall again to $V_{CC(UVLO)}$. This cycle is repeated until the junction temperature falls 8 degrees (typical) below $T_{prot(max)}$.

### 6.12 Burst standby mode

Pin CTRL and pin $I_{sense}$ are also used to implement the burst standby mode feature. In burst standby mode, the converter consumes less than 1 W (typical) of input power at a maximum output power of 100 mW. This power is sufficient to supply a low power device such as a microcontroller. Burst standby mode is entered when a current larger than the burst standby mode active current $I_{burst}$ is forced into pin CTRL, via the opto-coupler, for a period that is longer than the burst standby mode blanking period $t_{blank(burst)}$.

During a burst standby mode cycle, the soft-start capacitor $C_{SS}$, (see Fig.8) is charged to 1.25 V and then discharged via the soft-start resistor $R_{SS}$. When $C_{SS}$ is discharged to 0.5 V, a soft-restart is initiated. The frequency of a typical burst standby mode cycle is approximately: $\frac{1}{R_{SS} \times C_{SS}}$

If, during a burst standby mode cycle, the voltage at pin $V_{CC}$ falls below the trip level voltage $V_{CC(burst)}$, the IC will be supplied again from pin VIN. If $V_{CC(UVLO)}$ is reached within the burst cycle period due to an external load on pin $V_{CC}$, a restart cycle begins. If during a burst standby mode cycle, the voltage on pin $V_{CC}$ stays above the trip level voltage $V_{CC(burst)}$, a maximum burst efficiency is obtained because the IC is being consistently powered by the auxiliary winding.

### 6.13 Driver

The Gate of the external power MOSFET is driven from a driver circuit having a current sourcing capability of typically 100 mA, and a current sink capability of typically 500 mA. This permits fast turn-on and turn-off of the power MOSFET for efficient operation.

A low driver source current has been chosen in order to limit the $\Delta V/\Delta t$ at switch-on. This reduces Electro Magnetic Interference (EMI) and also limits the voltage spikes across the current sense resistor $R_{sense}$.

## 7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 2); positive currents flow into the chip; pin 1 is not allowed to be current driven. The voltage ratings are valid provided other ratings are not being violated; current ratings are valid provided the maximum power rating is not violated.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | voltage on pin $V_{CC}$ | continuous | –0.4 | +40 | V |
| $V_{CTRL}$ | voltage on pin CTRL | | –0.4 | +5 | V |
| $V_{DEM}$ | voltage on pin DEM | current limited | –0.4 | – | V |
| $V_{sense}$ | voltage on pin $I_{sense}$ | current limited | –0.4 | – | V |
| $V_{VIN}$ | voltage on pin VIN | | –0.4 | +550 | V |
| $I_{CTRL}$ | current on pin CTRL | $\delta < 10\%$ | – | 50 | mA |
| $I_{DEM}$ | current on pin DEM | | –250 | +250 | μA |
| $I_{sense}$ | current on pin $I_{sense}$ | | –1 | +10 | mA |
| $I_{DRIVER}$ | current on pin DRIVER | $\delta < 10\%$ | –0.8 | +2 | A |
| $I_{VIN}$ | current pin VIN | | – | +5 | mA |
| $P_{tot}$ | total power dissipation | $T_{amb} < 70$ °C | – | 0.75 | W |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $T_j$ | junction temperature | | –20 | +145 | °C |
| $V_{esd}$ | electrostatic discharge; | | | | |
| | human body model; note 1 | pins 1 to 6 (class II) | – | 2000 | V |
| | | pin 8 ($V_{in}$) (class I) | – | 1250 | V |
| | machine model; note 2 | | – | 200 | V |

**Notes**

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
2. Equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω resistor.

## 8 THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 100 | K/W |

## 9 QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611 part D"*.

## 10 CHARACTERISTICS

$T_{amb}$ = 25 °C; $V_{CC}$ = 15 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Start-up current source (pin VIN)** | | | | | | |
| $I_{VIN(min)}$ | minimum supply current drawn from pin VIN | $V_{CC} < V_{CC(trip)(VIN)}$, $V_{VIN} > 100$ V | 300 | 400 | 500 | µA |
| $V_{CC(VIN)trip}$ | supply voltage for pin VIN current trip level | $V_{VIN} > 100$ V | 0.5 | 0.75 | 1.0 | V |
| $I_{VIN(max)}$ | maximum supply current drawn from pin VIN | $V_{CC}$ = 10 V; $V_{VIN} > 100$ V | 1.25 | 1.6 | 1.95 | mA |
| $I_{VIN}$ | supply current drawn from pin VIN | after start-up; $V_{CC} > V_{CC(start)}$; $V_{VIN} > 100$ V | – | 100 | 300 | µA |
| $V_{bd}$ | breakdown voltage | | 550 | – | – | V |
| M-level | mains-dependent operation-enabling level | | 33 | 37 | 40 | V |
| $M_{UVLO}$ | mains undervoltage lock-out level | | 25 | 28.5 | 33 | V |
| **$V_{CC}$ management (pin $V_{CC}$)** | | | | | | |
| $V_{CC(start)}$ | start-up voltage | | 10.8 | 11.4 | 12 | V |
| $V_{CC(UVLO)}$ | undervoltage lock-out | | 8.5 | 9.0 | 9.5 | V |
| $V_{CC(hys)}$ | hysteresis voltage | $V_{CC(start)} - V_{CC(UVLO)}$ | 2.1 | 2.4 | 2.7 | V |
| $I_{CC(h)}$ | charging current (high) | $V_{VIN} > 100$ V; $V_{CC} < V_{CC(trip)(VIN)}$ | – | –0.25 | – | mA |
| $I_{CC(l)}$ | charging current (low) | $V_{VIN} > 100$ V; $V_{CC(trip)(VIN)} < V_{CC} < V_{CC(UVLO)}$ | –1.6 | –1.2 | –0.75 | mA |
| $I_{CC(restart)}$ | restart current | $V_{VIN} > 100$ V; $V_{CC(UVLO)} < V_{CC} < V_{CC(start)}$ | –1.25 | –1.0 | –0.75 | mA |
| $I_{CC(oper)}$ | supply current under normal operation | no load on pin DRIVER | – | 1.6 | – | mA |
| **Primary current simulation** | | | | | | |
| $\alpha_{PCS}$ | primary current simulation factor | | – | 0.9 | – | A.s/V |
| **Demagnetization management (pin DEM)** | | | | | | |
| $V_{th(DEM)}$ | demagnetization comparator threshold voltage | | 70 | 100 | 130 | mV |
| $I_{prot(DEM)}$ | demagnetization current | | –50 | – | –10 | nA |
| $V_{clamp(DEM)(neg)}$ | negative clamp voltage | $I_{(DEM)}$ = –150 µA | –0.5 | –0.25 | –0.05 | V |
| $V_{clamp(DEM)(pos)}$ | positive clamp voltage | $I_{(DEM)}$ = 250 µA | 0.55 | 0.7 | 0.85 | V |
| $t_{suppr}$ | suppression time of transformer ringing at start of secondary stroke | | 1.1 | 1.5 | 1.9 | µs |
| $V_{sc(prot)(DEM)}$ | short-circuit protection voltage | | –90 | –50 | –10 | mV |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Pulse width modulator** | | | | | | |
| $t_{on(min)}$ | minimum on-time | | – | 0 | – | |
| $t_{on(max)}$ | maximum on-time | latched | – | $1/f_{smps}$ | – | s |
| **Oscillator** | | | | | | |
| $f_{osc(min)}$ | minimum oscillator frequency | $V_{CTRL}$ > 1.5 V; no sync | – | 6 | – | kHz |
| $f_{osc}$ | oscillator frequency | $V_{CTRL}$ < 1.5 V; no sync; note 2 | 24 | 26 | 28 | kHz |
| $f_{smps(max)}$ | maximum SMPS switching frequency before frequency division | sync. on; note 3 | – | 54 | – | kHz |
| $f_{smps(hys)}$ | frequency hysteresis for division | sync. on | – | 4 | – | kHz |
| $V_{vco(start)}$ | voltage on pin CTRL where frequency reduction starts | sync off | 1.38 | 1.46 | 1.54 | V |
| $V_{vco(max)}$ | peak voltage on pin CTRL where frequency is equal to $f_{osc(min)}$ | sync off | – | 1.58 | – | V |
| **Duty cycle control (pin CTRL)** | | | | | | |
| $V_{CTRL(min)}$ | minimum voltage on pin CTRL for maximum duty cycle | | – | 1.0 | – | V |
| $V_{CTRL(max)}$ | maximum voltage on pin CTRL for minimum duty cycle | | – | 1.6 | – | V |
| $I_{prot(CTRL)}$ | current on pin CTRL | | –0.6 | –0.8 | –1.0 | µA |
| **Burst standby mode (pin CTRL)** | | | | | | |
| $V_{th(burst)(on)}$ | burst standby mode active threshold voltage | $I_{burst}$ = 4 mA | – | 3.6 | – | V |
| $I_{burst}$ | burst standby mode active current | | 4 | 7 | 11 | mA |
| $t_{blank(burst)}$ | burst standby mode blanking time | | 25 | 32 | 40 | µs |
| $V_{ch(sense)(burst)}$ | charge voltage on pin $I_{sense}$ in burst standby mode | | – | 1.25 | – | V |
| $V_{dis(sense)(burst)}$ | discharge voltage level on pin $I_{sense}$ in burst standby mode | | – | 0.5 | – | V |
| $I_{ch(sense)(burst)}$ | charging current into pin $I_{sense}$ in burst standby mode | | – | 100 | – | µA |
| $V_{CC(burst)}$ | supply voltage trip level for supply from pin VIN during burst standby mode | | – | 11.2 | – | V |
| $I_{CC(burst)}$ | supply current during burst standby mode | | – | 600 | – | µA |
| **Synchronization (pin CTRL)** | | | | | | |
| $V_{sync}$ | synchronization recognition voltage | | 0.37 | 0.52 | 0.65 | V |
| $\Delta V/\Delta t_{sync}$ | synchronization recognition | | – | 0.5(1) | – | V/µs |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Overcurrent and winding short-circuit protection (pin $I_{sense}$)** | | | | | | |
| $V_{sense(max)}$ | maximum source voltage for OCP | $f_{smps(min)}$; $\Delta V/\Delta t$ = 0.1 V/µs | 0.48 | 0.52 | 0.56 | V |
| | | $f_{smps(max)}$; $\Delta V/\Delta t$ = 0.1 V/µs | 0.33 | 0.37 | 0.41 | V |
| $t_{PD}$ | propagation delay from detecting $V_{sense(max)}$ to switch-off | $\Delta V/\Delta t$ = 0.5 V/µs | – | 140 | 185 | ns |
| $V_{swp}$ | winding short-circuit protection voltage | $\Delta V/\Delta t$ = 0.5 V/µs | 0.83 | 0.88 | 0.96 | V |
| $t_{leb}$ | blanking time for current and winding short-circuit protection | | 320 | 380 | 480 | ns |
| $I_{ss}$ | soft start current | $V_{sense}$ < 0.5 V | 45 | 60 | 75 | µA |
| $V_{ss(max)}$ | soft start maximum sense voltage | | 0.45 | 0.50 | 0.55 | V |
| **Overvoltage protection (pin DEM)** | | | | | | |
| $I_{OVP(DEM)}$ | OVP trigger current | see Section “Overvoltage protection” | 54 | 60 | 66 | µA |
| **Driver (pin DRIVER)** | | | | | | |
| $I_{source}$ | source current capability of driver | $V_{CC}$ = 9.5 V; $V_{DRIVER}$ = 5 V | – | –100 | –75 | mA |
| $I_{sink}$ | sink current capability of driver | $V_{CC}$ = 9.5 V; $V_{DRIVER}$ = 5 V | – | 500 | – | mA |
| | | $V_{CC}$ = 9.5 V; $V_{DRIVER}$ = 9.5 V | 400 | 700 | – | mA |
| $V_{o(driver)(max)}$ | maximum output voltage of driver | $V_{CC}$ > 12 V | – | 11.5 | 12 | V |
| **Temperature protection** | | | | | | |
| $T_{prot(max)}$ | maximum temperature protection level | | 130 | 140 | 150 | °C |
| $T_{prot(hys)}$ | hysteresis for the temperature protection level | | – | 8 | – | °C |

**Notes**

1. Guaranteed by design.
2. This is also the minimum SMPS switching frequency in synchronized mode.
3. This is also the maximum oscillator frequency in synchronized mode.

## 11 APPLICATION INFORMATION

A typical flyback converter that uses the TEA1541 consists of an input filter, a transformer with a third (auxiliary) winding, and an output stage with a feedback circuit.

Capacitor $C_{VCC}$ connected to pin $V_{CC}$ buffers the IC supply voltage from the rectified high voltage (AC) mains during start-up, or from the auxiliary winding during operation.

Resistor $R_{sense}$ converts the primary current into a voltage at pin $I_{sense}$. The resistor value defines the maximum primary peak current. Resistor $R_{SS}$ and capacitor $C_{SS}$ enable soft start and burst standby mode operation.

A resistor and a series diode can be placed in parallel with resistor $R_{DEM}$ to control the amount of current flowing into, and out of the IC, allowing the values of the OVP level and primary current simulation to be defined independently. More details are available in *Application note AN10205*.

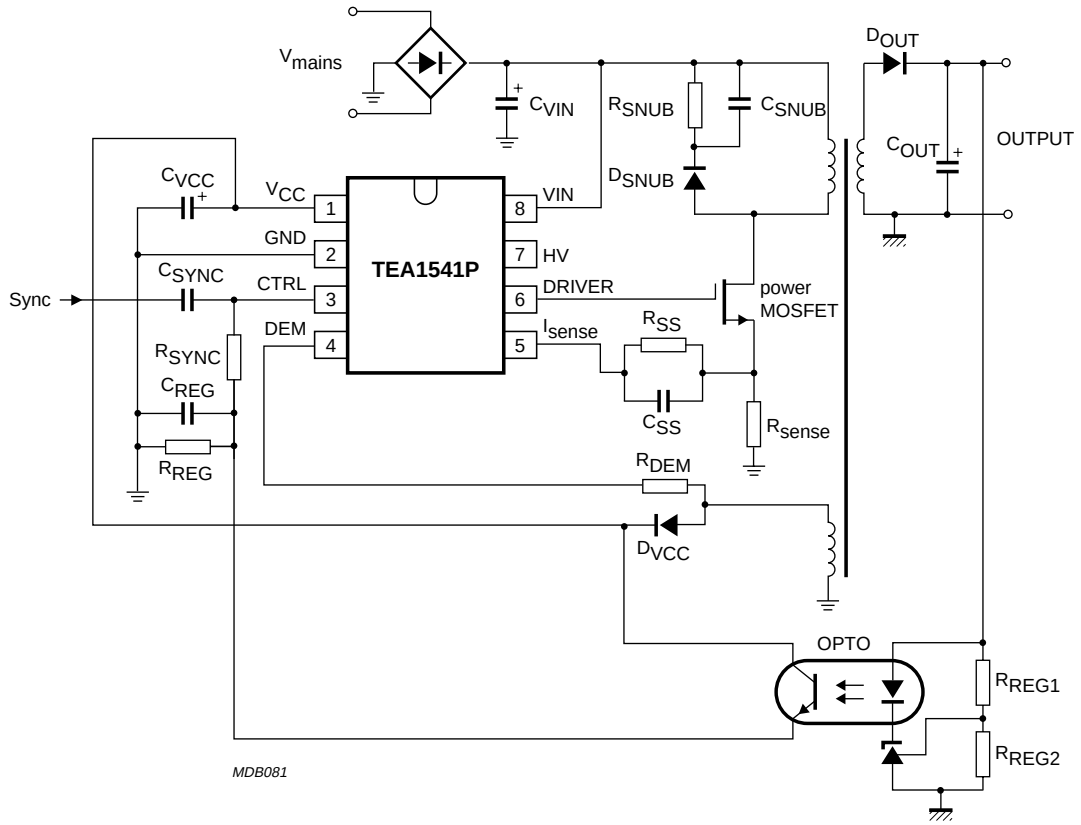
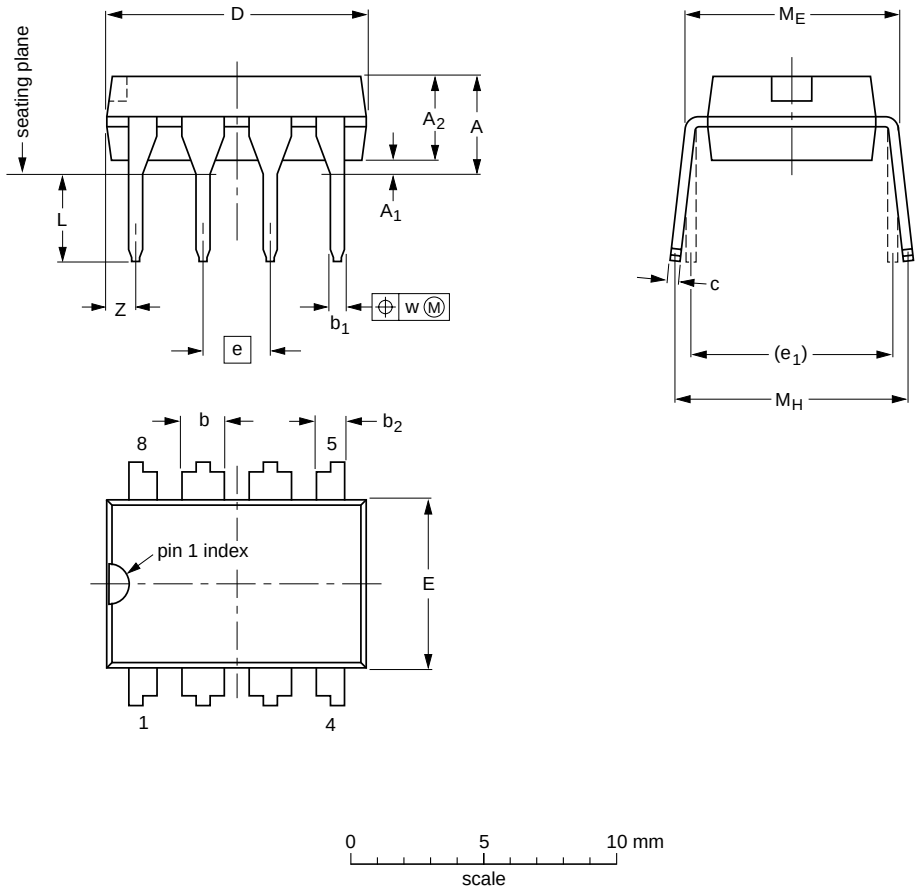



Fig.8 Flyback configuration with synchronization and soft start.

## 12 PACKAGE OUTLINE

**DIP8: plastic dual in-line package; 8 leads (300 mil)** **SOT97-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | $b_2$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.14 | 0.53<br>0.38 | 1.07<br>0.89 | 0.36<br>0.23 | 9.8<br>9.2 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 1.15 |
| inches | 0.17 | 0.02 | 0.13 | 0.068<br>0.045 | 0.021<br>0.015 | 0.042<br>0.035 | 0.014<br>0.009 | 0.39<br>0.36 | 0.26<br>0.24 | 0.1 | 0.3 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.045 |

**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT97-1 | 050G01 | MO-001 | SC-504-8 | | | ~~99-12-27~~<br>03-02-13 |

## 13 SOLDERING

### 13.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

### 13.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

### 13.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

### 13.4 Suitability of through-hole mount IC packages for dipping and wave soldering methods

| PACKAGE | SOLDERING METHOD | |
|---|---|---|
| | DIPPING | WAVE |
| DBS, DIP, HDIP, SDIP, SIL | suitable | suitable[1] |
| PMFP[2] | – | not suitable |

**Notes**

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
2. For PMFP packages hot bar soldering or manual soldering is suitable.

## 14 DATA SHEET STATUS

| LEVEL | DATA SHEET STATUS(1) | PRODUCT STATUS(2)(3) | DEFINITION |
|---|---|---|---|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| III | Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). |

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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